

REMARKS

Claims 1-22 are pending in the application. Claims 1, 13 and 22 have been amended. In view of the following, it is respectfully submitted that all of the currently unallowed claims are in condition for allowance.

Rejection of Claims 1, 4-10, 12-13, 16-19 and 21 Under 35 U.S.C. 102(b) As Being Anticipated By Schaper

Claim 1

Claim 1 recites a substrate of semiconductor material including a circuit integrally formed therein, an interconnection layer overlying the substrate and formed of a first conductive material, a distribution layer overlying the interconnection layer, the distribution layer including distribution grids, the distribution layer being formed of a second conductive material different from the first conductive material, and a plurality of connecting channels connecting selected ones of the distribution grids to selected locations of the interconnection layer.

For example, referring, *e.g.*, to FIGS. 1-2 and paragraphs 16-19 of the present application, an integrated circuit assembly 10 includes a processed semiconductor substrate 12, an interconnect layer 14, an insulator layer 16, and a distribution layer 18. The semiconductor substrate 12 has been processed to include an integrated circuit 22 diffused therein. The interconnect layer 14 is formed of a first conductor such as, for example, copper. The copper interconnection layer 14 overlies the substrate 12 and selectively makes electrical connection to the circuit 22 integrally formed in this substrate in a manner well known in the art. The interconnection layer 14 may make selective electroconnection to the circuit 22 through vias formed in an intervening insulative layer. Further, the interconnection layer may comprise a plurality of interspersed conductive layer patterns and oxide layers as are also known in the art. The distribution layer 18 is formed of a second conductive material which, for example, may preferably be aluminum.

Schaper, on the other hand, fails to teach the limitations recited in claim 1. Schaper, at, *e.g.*, FIGS. 1-6 and col. 5, lines 4-68 and col. 8, lines 1-68, teaches a

substrate 10 on which is formed a ground plane layer 11, a power plane distribution layer 13 and two signal layers 15 and 17, separated by various insulating layers 12, 14 and 16. A layer of silicon dioxide is applied to the surface of the substrate 10 to insulate the first metal layer 11 from the semiconducting silicon layer 10. The layer 11 typically is a continuous ground plane made of sputtered aluminum. Separating the ground plane 11 and the power distribution plane 13 is a thin layer of silicon dioxide 12. The power distribution layer 13 is applied in the same manner as the layer 11, and is likewise made of aluminum. In FIG. 6, illustrated is a base substrate 70 that carries an unpatterned insulating layer 71 thereover. Formed over the insulating layer 71 is a first metal layer 72. A dielectric insulating layer 73 is deposited over the first metal layer 72 and is employed to separate the layer 72 from a second metal layer 74. The dielectric insulating layer 73 is perforated with vias such as the via 79.

However, Schaper fails in any manner to teach that the substrates 10, 70 include a circuit integrally formed therein. Additionally, Schaper fails in any manner to teach or show that the vias 79 connect layer 72 to distribution layer 74. Moreover, Schaper fails to teach that the layers 11, 72 are formed of a first conductive material while the distribution layers 13, 74 are formed of a second conductive material different from the first conductive material.

Claim 13

Claim 13 is patentable for reasons similar to those discussed above in connection with claim 1.

Claims 4-10, 12, 16-19 and 21

Claims 4-10, 12, 16-19 and 21 are patentable by virtue of their respective dependencies from claims 1 and 13.

Rejection of Claims 1-3 and 13-15 Under 35 U.S.C. 102(b) As Being Anticipated
By Van Der Have

Claim 1

Claim 1 recites a substrate of semiconductor material including a circuit integrally formed therein, an interconnection layer overlying the substrate and formed of a first conductive material, and a distribution layer overlying the interconnection layer and formed of a second conductive material different from the first conductive material.

For example, referring, e.g., to FIGS. 1-2 and paragraphs 19-21 of the present application, the distribution layer 18 includes a plurality of wire bonding pads at its periphery including bonding pads 30, 32, 34, 36, and 38. The bonding pads 30 and 38 are electrically connected to the interconnection layer 14 through vias 31 and 39. The wire bonding pads 32, 34, and 36 are preferably similarly electrically connected to the interconnection layer 14 in this same manner. The distribution layer 18 is distributed essentially over the entire substrate 12 with distribution grids 50, 52, 54, 56, and 58.

van der Have, on the other hand, fails to teach the limitations recited in claim 1. van der Have, at, e.g., FIG. 12 and col. 26, line 50 to col. 27, line 20, teaches and shows a wafer 01 on which an overall circuit is fabricated. The wafer 01 includes a substrate wafer base region 57. The wafer 01 further has an interconnect system composed of three layers 46, 47 and 48, each of which are conductive films.

However, van der Have fails in any manner to teach that the substrate 57 includes a circuit integrally formed therein. Moreover, while van der Have does disclose a group of metals from which the conductive layer material may be chosen, van der Have fails to teach that the conductive material of any one of the layers 46, 47 and 48 must be different from the conductive material of another of the layers, as is required by claim 1.

Claim 13

Claim 13 as amended is patentable for reasons similar to those discussed above in connection with claim 1.

Claims 2-3 and 14-15

Claims 2-3 and 14-15 are patentable by virtue of their respective dependencies from claims 1 and 13.

**Rejection of Claims 20 and 22 Under 35 U.S.C. 103(a) As Being Unpatentable
Over Van Der Have In View of Lee**

Claim 20

Lee fails to supply the teachings missing from van der Have, namely a first metalization layer overlying a substrate and formed of a first metal, and a second metalization layer overlying the insulator layer and formed of a second metal different from the first metal. Accordingly, Lee and van der Have, taken either each alone or in combination, fail to teach or suggest the limitations recited in claim 13. As such, claim 20 is patentable by virtue of its dependency from claim 13.

Claim 22

Lee fails to supply the teachings missing from van der Have, namely a copper interconnection layer overlying a substrate, an insulator layer overlying the copper interconnection layer, and an aluminum distribution layer overlying the insulator layer. Accordingly, Lee and van der Have, taken either each alone or in combination, fail to teach or suggest the limitations recited in claim 22.

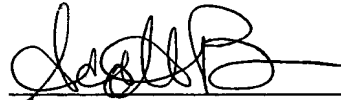
CONCLUSION

In view of the foregoing, Applicants believe that all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes that a

telephone conference would expedite prosecution of this application, please telephone the undersigned at (425) 455-5575. **If the Examiner does not agree that all pending claims are in condition for allowance, the Examiner is respectfully requested to contact the undersigned to arrange a discussion of the application prior to issuing an Office action.**

Respectfully submitted,
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